Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (canceled).

Claim 6 (previously presented): A device for CMOS electrostatic discharge input protection comprising:

a transistor with gate, source, drain and substrate terminals;

an input signal terminal coupled to said source terminal of said transistor;

a reference point coupled to said gate and substrate terminals of said transistor;

an output signal terminal coupled to said drain terminal of said transistor where under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and the leakage current of said transistor is reduced to below sub-threshold level while an increasing source voltage applied at said source terminal reduces the gate-to-source voltage and increases its threshold voltage said source voltage being a few 100mV; and

wherein said leakage current is approximately 10^{-14} A/um of transistor width.

Claims 7-14 (canceled).

Claim 15 (previously presented) A low leakage CMOS Electrostatic Discharge (ESD) protection scheme comprising:

a plurality of low operating voltage devices, each device having at least one device input for receiving an input signal;

a plurality of input terminals for coupling an input signal to a device via a corresponding device input;

a plurality of transistors with gate, substrate, source and drain terminals,

each transistor providing an alternate pathway via a source terminal for signals from said plurality of input terminals;

a reference coupled to corresponding gate and substrate terminals of said plurality of input protection transistors;

a source voltage driving both said source terminals of said input protection transistors and said inputs of said low operating voltage devices wherein under a non-ESD bias condition the leakage current of the input protection is greatly reduced due to reverse source bias and ESD protection is achieved by coupling the source terminals of said plurality of transistors to said plurality of input terminals thereby limiting the leakage current of each of said transistors to below sub-threshold level even as said source voltage increases, wherein said source voltage is limited to a few 100mV; and

wherein the resulting leakage current from said source voltage is approximately 10^{-14} A/um of transistor width.

Claims 16-24 (canceled).